NXP Makes Smart Connections Faster and More Reliable with New High Performance Wireless LAN Low Noise Amplifiers

NXP Semiconductors N.V. announced the introduction of its new wireless LAN LNAs with Integrated Switch that makes smart connections faster and more reliable on smartphones, tablets, wearables and small IoT devices. The company’s WLAN LNA+Switch family delivers stronger WLAN signals to offer a combination of high performance and low current functionality, making it possible for manufacturers to offer enhanced WLAN connectivity to help ensure the strongest signal available for consumers who want to be connected all the time, everywhere to share their experiences. The new Low Noise Amplifiers with Integrated Switch use higher throughput standards to enhance receive sensitivity for WLAN applications, including the latest 802.11ac 1Gb/s standard.

Manufactured using NXP’s high performance QUBiC eighth generation SiGe:C technology, the WLAN LNA+Switch family couples best-in-class noise figure, linearity and efficiency, and low insertion loss CMOS switches with the process stability and ruggedness that are the hallmarks of SiGe technology.

NXP’s WLAN LNA+Switches family that comprises BGS8324, BGS8358, BGS8424 and BGS8458 is available on reference designs from leading Mobile WLAN SoC suppliers.


IHP Reports Fastest Si-based Transistor at IEDM

At IEEE IEDM IHP presented the fastest silicon-based transistor in the world

Scientist Dr. Bernd Heinemann presented results on SiGe HBTs at the International Electron Devices Meeting (IEDM) in San Francisco.

“To present at IEDM is a valuable conclusion of the project ‘DOTSEVEN’, funded by the European Union. Together with Infineon and twelve other project partners from a total of six countries, the four-year project focused on developing SiGe HBTs with a maximum oscillation frequency, which is also referred to as fmax, of 0.7 THz,” says Dr. Bernd Heinemann, project manager at IHP.

“The presented fmax values exceed the best values of current production technologies by a factor of two. Such transistors enable the realization of wire-bound and wireless communication systems with even higher data rates (> 100 Gb/s).”

SiGe HBTs featuring fT/fmax/BVCEO = 505 GHz/720 GHz/1.6 V and a minimum CML ring oscillator gate delay of 1.34 ps were presented: “The improved speed derives from an optimized vertical profile, the combined application of millisecond annealing and a backend with low thermal budget, as well as lateral device scaling.

“With the fast HBTs the performance of radar systems, such as in personal cars, can be increased by reducing power consumption or increasing range and spatial resolution.”

In addition, the application becomes a reality in numerous new applications, which until now have been inaccessible to silicon components and which have been reserved for, compared to silicon technologies, the less integration-friendly solutions of III-V compound semiconductors. These newly emerging fields of application include imaging processes in the frequency range of 0.3 to 1 THz, which can be used for example for material testing, for safety inspections, for medical biopsies or for the detection of air pollution in the atmosphere.

It should be emphasized that these components are compatible with established silicon technologies and they are suitable as key elements for cost-effective systems in a broad market, he concludes.

WS: http://www.ihp-microelectronics.com
Pure-Play Foundry Market Surges 11% in 2016 to Reach $50 Bn
The pure-play foundry market is forecast to play an increasingly stronger role in the worldwide IC market during the next five years, according to IC Insights’ new 2017 McClean Report, which becomes available later this month. The 20th anniversary edition of The McClean Report forecasts that the 2016-2021 pure-play IC foundry market will increase by a compound annual growth rate (CAGR) of 7.6%; growing from $50.0 billion in 2016 to $72.1 billion in 2021.

IC foundries have two main customers—fabless IC companies (e.g., Qualcomm, Nvidia, Xilinx, AMD, etc.) and IDMs (e.g., ON, ST, TI, Toshiba, etc.). The success of fabless IC companies as well as the movement to more outsourcing by existing IDMs has fueled strong growth in IC foundry sales since 1998. Moreover, an increasing number of mid-size companies are ditching their fabs in favor of the fabless business model. A few examples include Fujitsu, IDT, LSI Corp. (now part of Avago), Avago (now Broadcom Ltd), and AMD, which have all become fabless IC suppliers over the past few years.

In 2016, the “Big 4” pure-play foundries (i.e., TSMC, GlobalFoundries, UMC, and SMIC) held an 85% share of the total worldwide pure-play IC foundry market. As shown, TSMC held a 59% marketshare in 2016, the same as in 2015, and its sales increased by $2.9 billion last year, more than double the $1.4 billion increase it logged in 2015. GlobalFoundries, UMC, and SMIC’s combined share was 26% in 2016, the same as in 2015.

The three top-10 pure-play foundry companies that displayed the highest growth rates in 2016 were X Fab (54%), which specializes in analog, mixed-signal, and high-voltage devices and acquired pure-play foundry Altis in 3Q16 to move into the top 10 for the first time, China-based SMIC (31%), and analog and mixed-signal specialist foundry TowerJazz (30%). Seven of the top 10 pure-play foundries are based in the Asia-Pacific region. Europe-headquartered specialty foundry X-Fab, Israel-based TowerJazz, and U.S.-headquartered GlobalFoundries are the only non-Asia-Pacific companies in the top 10 group.

SOTW: Terahertz spectroscopy and imaging of 3D semiconductors breaks the nanometer barrier
Researchers at Applied Research & Photonics (ARP; Harrisburg, PA) have broken the nanometer barrier for analysis of semiconductor layers in a 3D volume.1 The following is an excerpt with modifications from the paper describing the work performed: For many integrated circuit and high speed transistor applications the strain in the epitaxial layers of a semiconductor is relieved by introducing misfit dislocations that has inherent strain in their lattice structure.

Therefore, controlling the growth conditions and a strategic design of the structure is necessary for minimizing the density of dislocations threading through device layers grown on top of the relaxed buffer layer. While visualization of these structures on a nanometer scale is important, the time-domain spectroscopic investigation yields additional information about the molecular nature of these structures that are also important.

Gartner Says Worldwide Semiconductor Capital Spending Is Forecast to Grow 2.9 Percent in 2017
Worldwide semiconductor capital spending is projected to increase 2.9 percent in 2017, to $69.9 billion, according to Gartner, Inc. This is down from 5.1 percent growth in 2016 (see Table 1).

"The stronger growth in 2016 was fueled by Increased spending in late 2016 which can be attributed to a NAND flash shortage which was more severe in late 2016 and will persist though most of 2017. This is due to a better-than-expected market for smartphones, which is driving an upgrade of NAND spending in our latest forecast," said David Cirstensen, senior research analyst at Gartner. "NAND spending increased by $3.1 billion in 2016 and several related wafer fab equipment segments showed stronger growth than our previous forecast.

The thermal, track and implant segments in 2017 are expected to increase 2.5 percent, 5.6 percent and 8.4 percent, respectively. Compared with early 2016, the semiconductor outlook has improved, particularly in memory, due to stronger pricing and a better-than-expected market for smartphones. An earlier-than-anticipated recovery in memory should lead to growth in 2017 and be slightly enhanced by changes in key applications.

Foundries continue to outgrow the overall semiconductor market with mobile processors from Apple, Qualcomm, MediaTek and HiSilicon as the demand driver on leading-node wafers.

WS: http://www.icinsights.com

WS: http://www.laserfocusworld.com/articles/2017/01/terahertz
WS: http://www.gartner.com/technology/home.jsp

WS: http://www.icinsights.com
Global Semiconductor Sales Up 7 Percent Year-to-Year
The Semiconductor Industry Association (SIA), announced worldwide sales of semiconductors reached $31.0 billion for the month of November 2016, an increase of 7.4 percent compared to the November 2015 total of $28.9 billion and 2.0 percent more than the October 2016 total of 30.4 billion. November marked the market’s largest year-to-year growth since January 2015. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

“Global semiconductor sales continued to pick up steam in November, increasing at the highest rate in almost two years and nearly pulling even with the year-to-date total from the same point in 2015,” said John Neuffer, president and CEO, Semiconductor Industry Association. “The Chinese market continues to stand out, growing nearly 16 percent year-to-year to lead all regional markets. As 2016 draws to a close, the global semiconductor market appears likely to roughly match annual sales from 2015 and is well-positioned for a solid start to 2017.”

Month-to-month sales increased modestly across all regions: the Americas (3.3 percent), China (2.7 percent), Europe (2.5 percent), Asia Pacific/All Other (0.7 percent), and Japan (0.4 percent). Year-to-year sales increased in China (15.8 percent), Japan (8.2 percent), Asia Pacific/All Other (4.8 percent), and the Americas (3.2 percent), but fell slightly in Europe (-1.6 percent).

WS: http://www.semiconductors.org

SOTW: AMS AG Withdraws from NY Fab Project
AMS AG has withdrawn from a proposed wafer fabrication facility project with the state of New York. “We received a warm welcome from day one from the State of New York, the Utica community, Oneida County and Mohawk Valley EDGE,” said Alexander Everke, CEO of AMS. “The relationship with Mohawk Valley EDGE and Empire State Development was a very positive experience, and we remain open to future opportunities for cooperation. However, this decision was taken after thorough evaluation of the wafer fabrication project and its current status.”

The wafer fab project, based at Marcy in the Mohawk Valley in upstate New York, had already broken ground with a ceremony back in April 2016 but reports started to appear of problems and of a lack of activity on the site in December 2016. AMS was due to work in partnership with New York State and the State University of New York (SUNY) Polytechnic and the College of Nanoscience and Engineering (CNSE) to build, staff and operate the 200/300mm wafer fab.

Microsemi Unveils Six New Wideband, High Performance MMIC Products Covering DC-26 GHz for Defense and Industrial Markets
Microsemi announced six new MMIC products, including four wideband low noise MMIC amplifiers (MMA040AA, MMA041AA, MMA043AA and MMA044AA) and two wideband GaAs MMIC switches (MMS006AA and MMS008AA). The new MMIC products are suited for test and measurement, electronic warfare and radar applications.

Microsemi’s new devices are for a number of applications primarily within the defense and industrial markets, including receiver front end amplifiers for electronic warfare and signal intelligence; and wideband bench top and portable measurement equipment up to 26 GHz. Compared with existing market solutions, Microsemi’s new wideband low noise MMIC amplifiers deliver excellent performance with flat gain over a wide frequency range, and significantly better output third-order intercept point (OIP3) performance. Similarly, the new GaAs MMIC switches provide broad frequency coverage combined with superior insertion loss, isolation and input third-order intercept point (IIP3) performance. Global market research and consulting company Strategy Analytics estimates that GaAs MMICs sold into the EW, radar and microwave communications markets will reach $500 million by 2019.

WS: http://www.microsemi.com/existing-parts/part/137222

Skyworks Expands LTE Solutions for Internet of Things Applications
Skyworks Solutions, Inc unveiled its next generation LTE Category M-1 and NB-1 front-end solutions targeting machine-to-machine and Internet of Things applications requiring embedded cellular connectivity. Skyworks' newest multiband modules leverage half-duplex RF operation to deliver a highly integrated, turn-key solution that addresses Release 13 specifications of the 3GPP LTE standard - providing dependable, secure, low power connectivity in a compact package. These innovative products allow OEMs to simplify the design process, shorten development time, meet operator requirements worldwide and significantly accelerate time to market it said.

Skyworks Solutions also announced it has partnered with Libre Wireless, a leading embedded Wi-Fi and wireless technology and software solutions provider, to deliver the most advanced products for wireless audio and smart home applications. Libre Wireless is leveraging multiple solutions from Skyworks to enable their leading media modules targeting wireless audio, smart voice services and assistants, among other smart home applications.
SiGe News Review

NEWS BRIEFS

Microsemi was named the recipient of ZTE Corporation’s "2016 Best Delivery Support" award at ZTE’s Supplier Day event in Shenzhen, China. Microsemi received the award in recognition of its ability to consistently meet delivery schedule commitments and provide superior service and support.

GlobalWafers announced that the acquisition of SunEdison Semiconductor Ltd by GlobalWafers has been successfully completed. This follows GlobalWafers’ announcement on August 18, 2016 to acquire all outstanding ordinary shares of SunEdison Semiconductor in a transaction valued at US$683 m, a figure that includes SunEdison’s outstanding net debt.

SIA announced worldwide sales of semiconductors reached $30.5 billion for the month of October 2016, an increase of 3.4 percent from last month’s total of of global semiconductor companies that provide accurate and timely indicators of semiconductor trends.

TSMC announced consolidated revenue of NT$262.23 billion, net income of NT$100.20 billion, and diluted earnings per share of NT$3.86 (US$0.61 per ADR unit) for the fourth quarter ended December 31, 2016.

Faraday Technology Corp and Synopsys, Inc announced the expansion of Faraday’s design services to include a virtual prototyping solution. Faraday’s SoReal™ Virtual Platform.

Sequans Communications S.A. has leveraged its long-term partnership with TSMC, and TSMC’s ultra-low-power technology, to create Monarch, the first commercially available and most highly optimized LTE-M chip for the IoT.

ATopTech, Inc., an electronic design automation software company developing software solutions for engineers to assist them in the physical design of integrated circuits, announced that it has filed a voluntary petition under Chapter 11 of the Bankruptcy Code in the U.S. Bankruptcy Court for the District of Delaware.


Research and Markets has announced the addition of the "Global FinFET Technology Market, Analysis and Forecast: 2016 - 2022; Focus on 10nm, 14nm, 20nm FinFET; and Applications in Smart Phones and Wearable" report to their offering.

The global FinFET technology market is estimated to witness growth at a CAGR of 28.6% over the period of 2016 to 2022. This growth rate is expected due to increasing IC industry which is providing ample growth opportunities to FinFET market. The report is a compilation of different segments of global FinFET technology market including a market breakdown by technology, end user, and application. The report also discusses in detail about the key participants involved in the industry.

Partnerships, joint ventures, collaborations and contracts have also emerged as preferred strategies in bringing the FinFET technology market together. The companies with identical goals are collaborating together to form joint venture programmes in order to assist each other in achieving those goals. This helps companies gain access to each other’s technologies, services and thus facilitates them to achieve their objectives faster. Some of the key players involved in this market are Samsung Electronics Co, Ltd., Taiwan Semiconductor Manufacturing Company Limited, Intel Corporation, GlobalFoundries, United Microelectronics Corporation, Qualcomm Incorporated, ARM Ltd., SMIC and Xilinx Inc.

FinFET technology continues to gain immense popularity with increasing rate of revenue at a global level. Rising mobile and consumer electronics market and enhanced performance with lower current leakage has led to the widespread emergence of the global FinFET technology market.

North America led the global FinFET technology market in 2015. Asia Pacific FinFET technology market is expected to grow with the highest rate during the forecast period and overtake the position of North America in global FinFET technology market. China and India are going to be the key market regions for the growth of FinFET Technology in Asia Pacific region because of the growing demand of high end smartphones in the market. Large number of small and big companies are investing in smartphone market and this invariably leads to an increase in the growth of FinFET Technology market in this region.


SOTW: AMD Vega GPU Pictured Up Close, Biggest FinFET GPU by RTG

AMD has officially unveiled their Vega GPU to the masses at CES 2017. Along with the architectural preview, AMD also provided a glimpse at the Vega GPU die which will power the next-generation Radeon RX 500 series graphics cards.

The AMD Vega GPU was actually showcased to selected press at the AMD Tech Summit. The new graphics chip will be AMD’s first consumer aimed GPU to utilize the new HBM2 standard. This will allow them to double the capacity per die and clock per pin.

The increased density also allows AMD to cut down the costs in designing larger interposers. HBM2 itself takes more space compared to HBM1 with a die size around 92mm2 while HBM1 was just 35mm2 in size.

WS: http://wccftech.com/amd-vega-gpu-pictures-hbm2-official/
Tokyo Electron: 20160379842 (Kal; Subhadeep et al.) gas phase etching or method for dry removal of a material on a workpiece includes receiving a workpiece having a surface exposing a target layer composed of silicon and either (1) organic material or (2) both oxygen and nitrogen, and selectively removing at least a portion of the target layer from the workpiece. The selective removal includes exposing the surface of the workpiece to a chemical environment containing N, H, and F at a first setpoint temperature to chemically alter a surface region of the target layer, and then, elevating the temperature of the workpiece to a second setpoint temperature to remove the chemically treated surface region of the target layer.

TSMC: has applied for US Patent 20170012046 (Ching; Kuo-Cheng et al.) Method and Structure for FinFET Device describes a fin-like FinFET. The device includes one or more fin structures over a substrate, each with source/drain features and a high-k/metal gate (HK/MG). A first HK/MG in a first gate region wraps over an upper portion of a first fin structure, the first fin structure including an epitaxial silicon layer as its upper portion and an epitaxial growth SiGe, with a silicon germanium oxide (SiGeO) feature at its outer layer, as its middle portion, and the substrate as its bottom portion. A second HK/MG in a second gate region, wraps over an upper portion of a second fin structure, the second fin structure including an epitaxial SiGe layer as its upper portion, an epitaxial Si layer as its middle portion, and an epitaxial SiGe layer as its lower middle portion, and the substrate as its bottom portion.

Infineon Technologies Austria AG: 20170005171 (D Laforet, et al.) a Device Including a Contact Structure Directly Adjoining a Mesa Section and a Field Electrode includes a gate structure that extends from a first surface into a semiconductor portion and that surrounds a transistor section of the semiconductor portion. A field plate structure includes a field electrode and extends from the first surface into the transistor section. A mesa section of the semiconductor portion separates the field plate structure and the gate structure. A contact structure includes a first portion directly adjoining the mesa section and a second portion directly adjoining the field electrode. The first and second portions include stripes and are directly connected to each other.

IBM: (Bedell; Stephen W. et al.) has US Patent application 20160359044 for forming of dislocation-free SiGe FINFET using porous silicon—A device includes a semiconductor layer present on the porous core. The device may further include a strained semiconductor layer that is substantially free of defects that is present on the strained semiconductor layer. A gate structure may be present on a channel region of the fin structure, and source and drain regions may be present on opposing sides of the gate structure. Also, 20170005113 (K Cheng et al.) a method for forming CMOS devices includes masking a first portion of a tensile-strained silicon layer of a SOI substrate, doping a second portion of the layer outside the first portion and growing an undoped silicon layer on the doped portion and the first portion. The undoped silicon layer becomes tensile-strained. Strain in the undoped silicon layer over the doped portion is relaxed by converting the doped portion to a porous silicon layer to form a relaxed silicon layer. The porous silicon is converted to an oxide. A SiGe layer is grown and oxidized to convert the relaxed silicon layer to a compressed SiGe layer. Fins are etched in the first portion from the tensile-strained silicon layer and the undoped silicon layer and in the second portion from the compressed SiGe layer.

SAMSUNG ELECTRONICS: 20160379886 (Kim, Dong-Kwon; et al.) a method for fabricating a device includes forming a pre-fin extending in a first direction, the pre-fin including first, second, and third regions, forming first and second gates on the pre-fin to extend in a second direction intersecting the first direction, the first and second gates being spaced apart from each other in the first direction and overlapping with the first and second regions, respectively, forming first and second dummy spacers on the first and second regions, respectively to form a first trench in the third region that exposes the third region, forming a second trench by etching the exposed third region using the first and second dummy spacers as masks to separate the pre-fin into first and second active fins corresponding to the first and second regions, respectively, forming a dummy gate by filling the first and second trenches and removing the first and second dummy spacers.

Varian Semiconductor: 20160379832 (S Ruffell) a FINFET space etch with no fin recess may include providing a patterned feature extending from a substrate plane of a substrate, the patterned feature including a semiconductor part and a coating in an unhardened state extending along a top region and along sidewall regions; implanting first ions into the coating, the first ions having a first trajectory along a perpendicular to the substrate plane, wherein the first ions form a etch-hardened portion comprising a hardened state disposed along the top region; and directing a reactive etch using second ions at the coating, the second ions having a second trajectory forming a non-zero angle with respect to the perpendicular, wherein the reactive etch removes the etch-hardened portion at a first etch rate.
TSMC: 20160379831 (Yeo; Yee-Chia et al.) Multi-Gate Field Effect Transistors Having Oxygen-Scavenged Gate Stack A method includes forming a silicon cap layer on a semiconductor fin, forming an interfacial layer over the silicon cap layer, forming a high-k gate dielectric over the interfacial layer, and forming a scavenging metal layer over the high-k gate dielectric. An anneal is then performed on the silicon cap layer, the interfacial layer, the high-k gate dielectric, and the scavenging metal layer. A filling metal is deposited over the high-k gate dielectric.

INTEL: 20160372607 (Le; Van H. et al.) for strain compensation in transistors includes a device comprising: a first epitaxial layer, coupled to a substrate, having a first lattice constant; a second epitaxial layer, on the first layer, having a second lattice constant; a third epitaxial layer, contacting an upper surface of the second layer, having a third lattice constant unequal to the second lattice constant; and an epitaxial device layer, on the third layer, including a channel region; wherein (a) the first layer is relaxed and includes defects, (b) the second layer is compressive strained and the third layer is tensile strained, and (c) the first, second, third, and device layers are all included in a trench.

Application 20170004962: (Park, et al.) of “U.S.A. as represented by the Administrator of the National Aeronautics and Space Administration” a double sided hybrid crystal structure including a trigonal Sapphire wafer containing a (0001) C-plane and having front and rear sides. The Sapphire wafer is substantially transparent to light in the visible and infrared spectra, and also provides insulation with respect to RF noise. A layer of crystalline Si material having a cubic diamond structure aligned with the cubic <111> direction on the (0001) C-plane and strained as rhombohedron to thereby enable continuous integration of a selected (SiGe) device onto the rear side of the Sapphire wafer. The double sided hybrid crystal structure further includes an integrated III-Nitride crystalline layer on the front side of the Sapphire wafer that enables continuous integration of a selected III-Nitride device on the front side of the Sapphire wafer.

STMicroelectronics: 20160380087 (Q Liu) lateral BJT on a SOI substrate—a transistor is supported by a substrate including a semiconductor layer overlying an insulating layer. A transistor base is formed by a base region in the semiconductor layer that is doped with a first conductivity type dopant at a first dopant concentration. The transistor emitter and collector are formed by regions doped with a second conductivity type dopant and located adjacent opposite sides of the base region. An extrinsic base includes an epitaxial layer in contact with a top surface of the base region. The epitaxial layer is doped with the first conductivity type dopant at a second dopant concentration greater than the first dopant concentration. Sidewall spacers on each side of the extrinsic base include an oxide liner on a side of the epitaxial layer and the top surface of the base region.

GLOBALFOUNDRIES: 20160372598 (Yun-Yu Wang; et al.) for generating tensile strain in bulk FINFET channel; a method of forming fin-type transistors. The method includes forming a finFET structure having a fin channel region underneath a gate structure, and a source region and a drain region directly adjacent to the fin channel region at two opposing sides of the gate structure; and subjecting the source region and the drain region to a compressive strain; thereby causing the source region and the drain region to exert a tensile strain to the fin channel region. A finFET transistor formed thereby is also provided, which includes a channel region of fin shape covered by a gate on top thereof; a source next to a first end of the channel region on a first side of the gate; and a drain next to a second end of the channel region on a second side of the gate, wherein the source and drain are made of epitaxially grown SiGe having a Ge concentration level of at least 50% atomic percentage covered with silicon cap.
SiGe News Review

Global News Headlines

Page

nFET Si layer. SiGe layer of a third concentration is in plane with the grown SiGe layer of a third concentration in the pFET, where the second Ge concentration.

Then, growing a silicon layer over the SGOI in the nFET and recessing the SiGe in the pFET to a second Ge concentration and removing the first oxide layer over the pFET. Then, increasing the first Ge concentration in the SiGe layer and pFET, where the strained material stack forming a metal-silicide layer.

Commissariat a l'Energie Atomique et aux Energies Alternatives: 9,536,951 (Maitrejean, et al.) for a FinFET transistor comprising portions of SiGe with a crystal orientation [111] FinFET transistor comprising at least: one fin that forms a channel, a source and a drain, comprising an alternating stack of first portions of silicon-rich SiGe and of second portions of a dielectric or semiconductor material, and third portions of germanium-rich SiGe arranged at least against lateral faces of the first portions, one gate that covers the channel, and wherein each one of the third portions comprises faces with a crystal orientation [111] covered by the gate.

GLOBALFOUNDRIES: 9,525,027 (Hashemi, et al.) lateral bipolar junction transistor having graded SiGe base. A lateral bipolar junction transistor is fabricated using a SOI substrate. The transistor includes a germanium gradient within a doped silicon base region, there being an increasing germanium content in the direction of the collector region of the transistor. The use of a substrate including parallel silicon fins to fabricate lateral bipolar junction transistors facilitates the inclusion of both CMOS FinFET devices and lateral bipolar junction transistors having graded silicon germanium base regions on the same chip.

IBM: 9,536,736 (Bedell, et al.) reducing substrate bowing caused by high percentage SiGe layers. This relates to a structure and method for reducing substrate bowing resulting from the formation of strained SiGe layers having a high percentage of germanium ("high concentration SiGe") on silicon substrates. During the epitaxial growth of the high concentration SiGe layer, carbon dopant atoms may be introduced to the crystalline lattice structure of the SiGe, forming a SiGe:C layer. The carbon dopant atoms may reduce tensile strain in the SiGe:C layer during annealing, thereby reducing substrate bowing. See also, 9,543,888 (Lauer, et al.) complementary metal-oxide silicon having silicon and silicon germanium channels. A SGOI wafer having nFET and pFET regions is accessed, the SGOI wafer having a SiGe layer having a first germanium concentration, and a first oxide layer over nFET and pFET and removing the first oxide layer over the pFET. Then, increasing the first Ge concentration in the SiGe layer in the pFET to a second Ge concentration and removing the first oxide layer over the nFET. Then, recessing the SiGe layer of the first Ge concentration in the nFET so that the SiGe layer is in plane with the SiGe layer in the pFET of the second Ge concentration.

Then, growing a silicon layer over the SGOI in the nFET and a SiGe layer of a third concentration in the pFET, where the SiGe layer of a third concentration is in plane with the grown nFET Si layer.

Awarded Patents I

NATIONAL SEMICONDUCTOR: 9,543,296 (Vashchenko) an ESD clamp with auto biasing under high injection conditions. In a dual direction ESD protection circuit formed from multiple base-emitter fingers that include a SiGe base region, and a common sub-collector region, the I-V characteristics are adjusted by including P+ regions to define SCR structures that are operable to sink positive and negative ESD pulses, and adjusting the layout and distances between regions and the number of regions.

TSMC: 9,536,771 (Chen, et al.) gap fill self planarization on post epi—IC having transistors with structures separated by a flowable dielectric material, and a related method of formation. In some embodiments, an integrated chip has a semiconductor substrate and an embedded SiGe region extending as a positive relief from a location within the semiconductor substrate to a position above the semiconductor substrate. A first gate structure is located at a position that is separated from the embedded SiGe region by a first gap. A flowable dielectric material is disposed between the gate structure and the embedded SiGe region and a pre-metal dielectric (PMD) layer disposed above the flowable dielectric material. The flowable dielectric material provides for good gap fill capabilities that mitigate void formation during gap fill between the adjacent gate structures. See also, 9,543,438 (Tsai, et al.) contact resistance reduction technique—method of manufacturing a semiconductor device, the method including forming a first gate over a substrate, forming a recess in the substrate adjacent the first gate, epitaxially forming a strained material stack in the recess, the strained material stack comprising at least three layers, each of the at least three layers comprising a dopant. The method further includes co-implanting the strained material stack with dopants comprising boron, germanium, indium, tin, or a combination thereof, forming a metal layer on the strained material stack, and annealing the metal layer and the strained material stack forming a metal-silicide layer. 9,543,419 (Fan, et al.) FinFET structures forming an epitaxial including a III-V material. A damaged material layer being on at least one surface of the epitaxial portion. The method further including oxidizing at least outer surfaces of the damaged material layer to form an oxide layer, selectively removing the oxide layer, and repeating the oxidizing and the selectively removing steps.
STMicroelectronics: 9,543,304 (Liu, et al.) Vertical junction FinFET device and method for manufacture. A vertical JFET is supported by a semiconductor substrate that includes a source region within the semiconductor substrate doped with a first conductivity-type dopant. A fin of semiconductor material doped with the first conductivity-type dopant has a first end in contact with the source region and further includes a second end and sidewalls between the first and second ends. A drain region is formed of first epitaxial material grown from the second end of the fin and doped with the first conductivity-type dopant. A gate structure is formed of second epitaxial material grown from the sidewalls of the fin and doped with a second conductivity-type dopant.

CYMER, LLC: 9,541,840 (Brandt, et al.) aceted EUV optical element. A reflective EUV optic such as a collector mirror configured as an array of facets that are spaced apart to form respective gaps between adjacent facets. The gaps are used as inlets for gas flow across one of the facets such that flow is introduced parallel to the optic surface. The facets can be made with offsets such that loss of reflective area of the EUV optic can be minimized. The gas facilitates removal of target material from the surface of the facets.

GLOBALFOUNDRIES: 9,543,216 (Niimi, et al.) Integration of hybrid germanium and group III-V contact epilayer in CMOS. A trench contact epilayer in a semiconductor device is provided. Embodiments include forming trenches through an interlayer dielectric (ILD) over source/drain regions in NFET and PFET regions; depositing a conformal silicon nitride layer over the ILD and in the trenches; removing the SiN layer in the PFET region; growing a germanium epilayer over the source/drain regions in the PFET region; depositing metal over the ILD and in the trenches in the NFET and PFET regions; etching the metal in the NFET region to expose the conformal SiN layer; removing the SiN layer in the NFET region; growing a Group III-V epilayer over the source/drain regions in the NFET region; and depositing metal over the ILD and in the trenches in the NFET region.

Altera: 9,543,382 (W Wu, et al.) FinFET with improved SEU performance. Illustratively, a finFET comprises at least one fin, and typically several fins, with a trapping region in or on a substrate at the base of each fin to trap ions produced by radiation incident on the substrate. In one embodiment, the trapping region is an implanted region having a conductivity type opposite that of the substrate or by creating defects in the substrate or by epitaxially growing a region or regions having an opposite conductivity type to that of the substrate.

IBM: 9,543,323 (Cheng, et al.) strain release in PFET regions. A method for fabricating a semiconductor device, includes providing a strained silicon on insulator (SSOI) structure, the SSOI structure comprises, a dielectric layer disposed on a substrate, a silicon germanium layer disposed on the dielectric layer, and a strained semiconductor material layer disposed directly on the silicon germanium layer, forming a plurality of fins on the SSOI structure, forming a gate structure over a portion of at least one fin in a nFET region, forming a gate structure over a portion of at least one fin in a pFET region, removing the gate structure over the portion of the at least one fin in the pFET region, removing the silicon germanium layer exposed by the removing, and forming a new gate structure over the portion of the at least one fin in the pFET region, such that the new gate structure surrounds the portion on all four sides.

SMIC: 9,543,411 (Cai, et al.) LDMOS transistor includes a semiconductor substrate having a well region and a drain region in the well region. The LDMOS transistor also includes at least one drifting region in the well region and an annular source region in the drifting region surrounding the drain region. Further, the LDMOS transistor includes at least one annular isolation structure surrounding the drain region in the drifting region. Further, the LDMOS transistor also includes an annular gate dielectric layer on the well region and an annular gate on the annular gate dielectric layer.

UMC: 9,543,203 (Lu, et al.) fabricating a structure with self-aligned contact includes the steps: forming a first interlayer dielectric on a substrate; forming a gate electrode on the substrate so that the periphery of the gate electrode is surrounded by the first interlayer dielectric; forming a conformal dielectric layer to conformally cover the layer of organic material; and forming a second interlayer dielectric to cover the conformal dielectric layer.

ASM IP Holding: 9,543,180 (Kamiya) apparatus and method for transporting wafers between wafer carrier and process tool under vacuum: a chamber for carrier with front opening with cover; rotatable platform for placing carrier in chamber and opening/closing device for cover; platform rotates to set the wafer carrier at the first position and a second position for transporting a wafer to a wafer-handling chamber.
SEMICON Korea 2017
To be held from February 8 to 10 and be the largest in its 30 year history it says. Held in COEX Seoul, Korea.  
WS: http://www.semiconkorea.org/en

ISSCC 2017
WS: http://isscc.org

EDTM 2017
28 February - 2 March 2017  
IEEE Electron Devices Technology and Manufacturing Conference Toyama International Conference Center, Japan  
WS: http://ewh.ieee.org/conf/edtm/2017

SEMICON China 2017
To be held from March 14 - 16, 2017 at the Shanghai New International Expo Centre.  
WS: http://www.semiconchina.org/

EUROSOI Workshop
To be held from 3 - 5 April, the 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS) will be held at the Institute of Nanoscience & Nanotechnology of NCSR 'Demokritos', Athens, Greece.  
E-mail: a.nasiopoulou@inn.demokritos.gr  
WS: http://www.eurosoi-ulis2017.inn.demokritos.gr

SEMICON SE Asia 2017
To be held from April 25-27 at the SPICE Arena Penang, Malaysia.  
WS: http://www.semiconsea.org/

ITF Belgium
To be held from 16 - 17 May, the Imec Technology Forum 2017 in Antwerp, Belgium.  
WS: http://www2.imec.be/be_en/events.html

FUTURE ENTRIES
If your meeting has not appeared here please email me as soon as possible for inclusion in the next issue.

Purdue demos potential of beta gallium oxide on insulator transistor for ultra-efficient switches in power electronics
Purdue University has demonstrated the high-performance potential of an experimental transistor made of beta gallium oxide, which could bring new ultra-efficient switches for applications such as the power grid, military ships and aircraft. (Hong Zhou et al, 'High Performance Depletion/Enhancement-Mode beta-Ga2O3 on Insulator (GOOI) Field-effect Transistors with Record Drain Currents of 600/450mA/mm\(^2\), IEEE Electron Device Letters, vol38 (2017), no1, p103). These drain currents are nearly one order of magnitude higher than any other reported ID values. The GOOI FET is promising because it has an ultra-wide bandgap as needed for switches in high-voltage applications. Compared with other semiconductors, devices made from b-Ga2O3 have a higher breakdown voltage, says Peide Ye, Purdue University’s Richard J. and Mary Jo Schwartz Professor of Electrical and Computer Engineering.  
The team explains that threshold voltage can be modulated by varying the thickness of the b-Ga2O3 films and the E-mode GOOI FET can be achieved by shrinking the b-Ga2O3 film thickness. Benefiting from the good interface between b-Ga2O3 and SiO2 and wide bandgap of b-Ga2O3, negligible transfer characteristic hysteresis, high ID on/off ratio of 1010, and low subthreshold swing of 140 mV/dec for a 300 nm thick SiO2 are observed. E-mode GOOI FET with source to drain spacing of 0.9 um demonstrates a breakdown voltage of 185 V and an average electric field (E) of 2 MV/cm, showing the great promise of GOOI FET for future power devices. The research was based at Discovery Park’s Birck Nanotechnology Center.  
WS: http://www.purdue.edu/  
A copy of the research paper is available from Emil Venere, Purdue News Service, at 765-494-4709, venere@purdue.edu
NEW BOOKS....

**Introduction to the Physics of Silicene and other 2D Materials (Lecture Notes in Physics)**

Springer by Seymur Cahangirov et al. The text starts with a brief history of silicene, followed by a comparison of the bonding nature in silicon versus carbon atoms. Here, a simple but robust framework is established to help the reader follow the concepts presented throughout the book. The book then presents the atomic and electronic structure of freestanding silicene, followed by an account of the experimental realization of silicene on substrates. 


**Silicon Earth Second Edition**

The new “Silicon Earth: Introduction to Microelectronics and Nanotechnology, Second Edition” (CRC PRC Press) by John D. Cressler, Georgia Institute of Technology(ISBN: 9781498708258) 595 Pages, 557 in color, introduces readers with little or no technical background to the marvels of microelectronics and nanotechnology, using straightforward language, an intuitive approach, minimal math, and lots of pictures. The general scientific and engineering underpinnings of microelectronics and nanotechnology are described, as well as how this new technological revolution is transforming a broad array of interdisciplinary fields, and civilization as a whole.

*WS: http://tinyurl.com/hr20ozj

**Nanoscale Silicon Devices**

A book by Shunri Oda and David K. Ferry, 288 Pages - 16 Color & 190 B/W Illustrations ISBN 9781482286760 - CAT# K22593 provides an introduction to new concepts (including variability in scaled MOSFETs, thermal effects, spintronics-based nonvolatile computing systems, spin-based qubits, magnetoelectric devices, NEMS devices, tunnel FETs, dopant engineering, and single-electron transfer), new materials (such as high-k dielectrics and germanium), and new device structures in three dimensions.

*WS: http://tinyurl.com/j755xpe
Google Books: http://tinyurl.com/jumuyjz

**Book Covers Entire Spectrum of R&D in Si, Ge, and SiGe Alloys**

Edited by Gudrun Kissinger, Innovations for High Performance Microelectronics, Frankfurt (Oder), Germany and Sergio Pizzini, University of Milano-Bicocca, Italy, it covers crystal growth, point defects, extended defects, and impurities of Si and Ge nanocrystals, and chapters, span bulk, thin film, and nanostructured materials growth and characterization problems, theoretical modeling, crystal defects, diffusion, and issues of key applicative value, including chemical etching as a defect delineation technique, the spectroscopic analysis of impurities, and the use of devices as tools for the measurement of materials quality.

*WS: http://tinyurl.com/mousupn
Preview: http://www.amazon.co.uk/Silicon-Germanium-Their-Alloys-Nanocrystals/dp/1466586648

**CMOS Circuits for Electromagnetic Vibration Transducers**

A new book by Authors: Maurath, Dominic, Manoli, Yiannos University of Freiburg, Germany. Three comprehensive parts - the book addresses interfaces for energy harvesting, which are the key element to connect the micro transducers with energy storage. Chip-integrated power management solutions are a must for ultra-low power systems. This enables not only the optimization of innovative sensor applications. It is also essential for integration and miniaturization of energy harvesting supply strategies of portable and autonomous monitoring systems.


**CMOS 60-GHz and E-band Power Amplifiers and Transmitters**

Authors: Zhao, Dixin, Reynaert, Patrick

This book focuses on the development of design techniques and methodologies for 60-GHz and E-band power amplifiers and transmitters at device, circuit and layout levels. The authors show the recent development of millimeter-wave design techniques, especially of power amplifiers and transmitters, and presents novel design concepts, such as “power transistor layout” and “4-way parallel-series power combiner”, that can enhance the output power and efficiency of power amplifiers in a compact silicon area. Five state-of-the-art 60-GHz and E-band designs with measured results are demonstrated to prove the effectiveness of the design concepts and hands-on methodologies presented. This book serves as a valuable reference for circuit designers to develop millimeter-wave building blocks for future 5G applications.


**Ultra-Low-Power & Ultra-Low-Cost Short-Range Receivers in Nanoscale CMOS**

Authors: Lin, Zhiheng, Mak (Elvis), Pui-In, Martins, Rui Paulo. Provides readers with a description of techniques to be used for ULP and ultra-low-cost, short-range wireless receivers and what is required to deploy these receivers in short-range wireless sensor networks, which are proliferating widely to serve the IoT for “smart cities.”


COMING SOON:

**Silicon-Based Photonics (Pan Stanford)** by Erich Kasper & Jingzhong Yu (Editors) will be released on February 4, 2018. Covers basics of band structure of silicon and germanium and their influence on photonic properties and discusses system layout and key device components with the application background in mind. Special focus is given to SOI-based interconnects and passive waveguide devices and to Ge-on-Si heterostructure devices for light detection, modulation, and emission.

**Material Design of Metal/Oxide Interfaces for Nanoelectronics Applications (NIMS Monographs)** out next June from Springer by Takahiro Nagata. Investigation and intentional control of metal/oxide interface structure and electrical properties with the data obtained using non-destructive methods such as XPS and XRR are discussed. Oxide materials should support the development of future functional devices with High-k, ferroelectric, magnetic and optical properties.
**SiGe News Review**

**Extreme Environment Electronics**  
*Written by J.D. Cressler and Alan Mantooth. Published by CRC Press.*  
This book ranges from the extreme environments themselves, to basic physics of the various interactions between devices and environments, the detailed aspects of electronic design, modeling of devices through systems, packaging design, reliability and QA, to ultimately a wide class of end-use applications intended for real extreme environments.  

**Automatic Gain Control: Techniques and Architectures for RF Receivers (Analog Circuits and Signal Processing)**  
*Written by Juan Pablo Alegre Pérez, Santiago Celma Pueyo and Belén Calvo López. Published by Springer.*  
This book analyzes AGC loop circuits and demonstrates AGC solutions in the environment of wireless receivers, mainly in wireless receivers with stringent constraints in settling-time and wide dynamic range, such as WLAN and Bluetooth receivers.  

**Impact des perturbations électromagnétiques sur les composants Si/SiGe: Le Transistor Bipolaire à Hétérojonction Si/SiGe sous contraintes ... à l'analyse structurale (French Edition)**  
*Written by Ali Aledidine. Published by Editions universitaires europeennes.*  
This work proposes a new methodology for the study of the reliability of THBS SiGe technology. The originality of this study is the use of an electromagnetic stress effective and targeted with the bench near field. Static characterizations showed the presence of leakage currents at the interface Si/SiO2.  

**Strain-Induced Effects in Advanced MOSFETs**  
*Written by Viktor Sverdlov. Published by Springer.*  
The book covers all relevant modeling approaches used to describe strain in silicon. The subband structure in stressed semiconductor films is investigated in devices using analytical k.p and numerical pseudopotential methods. A rigorous overview of transport modeling in strained devices is given.  

**Terahertz Radiation: High-impact Emerging Technology - What You Need to Know: Definitions, Adoptions, Impact, Benefits, Maturity, Vendors**  
*Written by Kevin Roebuck. Published by Tebbo.*  
In easy to read chapters, with extensive references and links to get you to know all there is to know about Terahertz Radiation right away.  

**Black silicon germanium (SiGe) for extended wavelength near infrared electro-optical applications.**  
*Published by Books LLC, Reference Series (October 6, 2011).*  
*WS: [http://www.amazon.com/germanium-extended-wavelength-e electro-optical-applications/dp/1234546582/ref=sr_1_1?ie=UTF8&qid=1318614903&sr=8-1]*

**Silicon-Germanium (SiGe) Nanostructures: Production, Properties and Applications in Electronics**  
*Written by Y. Shiraki (Author, Editor), N. Usami (Editor). Published by Woodhead Publishing Ltd.*  
Reviews the materials science of nanostructures and their properties and applications in different electronic devices; assesses the structural properties of SiGe nanostructures, discussing electronic band structures of SiGe alloys; explores the formation of SiGe nanostructures featuring different methods of crystal growth such as molecular beam epitaxy and chemical vapour deposition.  
*WS: [http://www.amazon.co.uk/Silicon-Germanium-SiGe-Nanostructures-Applications-Electronics/dp/1845696891/ref=sr_1_18?ie=UTF8&qid=1289072797&sr=8-1]*

**Compact Hierarchical Bipolar Transistor Modeling with Hicum (International Series on Advances in Solid State Electronics & Technology)**  
*Written by: Michael Schröter and Anjan Chakravorty. Published by World Scientific Publishing Co Pte Ltd.*  
Compact Hierarchical Bipolar Transistor Modeling with Hicum will be of great practical benefit to professionals from the modelling, circuit design, and process development community who are interested in SiGeC HBTs fabricated with existing cutting-edge process technology.  
*WS: [http://www.amazon.co.uk/Hierarchical-Bipolar-Transistor-Mo delling-Hicum/dp/981427321X/ref=sr_1_18?ie=UTF8&qid=1289072797&sr=8-1]*

**Silicon Earth : Introduction to the Microelectronics and Nanotechnology Revolution**  
*Written by J.D. Cressler Published by Cambridge University Press, New York.*  
Silicon Earth introduces readers with little or no technical background to the many marvels of microelectronics and nanotechnology, using easy, non-intimidating language and an intuitive approach with minimal math. The general scientific and engineering underpinnings of microelectronics and nanotechnology are addressed.  

**Technology Computer Aided Design for Si, SiGe and GaAs Integrated Circuits**  
*Written by GA Armstrong and CK Maiti. Published by IET Circuits, Devices and Systems.*  
The first book that deals with a broad spectrum of process and device design, and modelling issues related to various semiconductor devices. This monograph attempts to bridge the gap between device modelling and process design using TCAD. Examples for types of Si-, SiGe-, GaAs- and InP-based heterostructures, this book presents a comprehensive perspective of emerging fields and covers topics ranging from materials to fabrication, devices, modelling and applications.  
*WS: [http://www.amazon.co.uk/Technology-Computer-Aided-Design/dp/0863417455/ref=sr_1_18?ie=UTF8&qid=1277940142&sr=8-1]*

**Analysis and Design of Monolithic Integrated SiGe Mixer Circuits for 77GHz Automotive Radar**  
*Written by Marcus Hartmann. Published by Berichte Aus Der Halbleitertechnik.*  
*WS: [http://www.amazon.co.uk/Analysis-Monolithic-Integrated-Automotive/dp/3832270876/ref=sr_1_17?ie=UTF8&qid=1277940275&sr=8-1]*


**WS: [http://www.amazon.com/Automatic-Gain-Control-Techniques-Architectures/dp/1461401666/ref=sr_1_8?ie=UTF8&qid=1318615013&sr=8-1&keywords=automatic+gain+control]**


**WS: [http://www.amazon.com/Strain-Induced-Effects-Advanced-Computational-Microelectronics/dp/3709103819/ref=sr_1_17?ie=UTF8&qid=1318614896&sr=8-1]**


**WS: [http://www.amazon.com/germanium-extended-wavelength-electro-optical-applications/dp/1234546582/ref=sr_1_1?ie=UTF8&qid=1318614903&sr=8-1]**

**WS: [http://www.amazon.co.uk/Silicon-Germanium-SiGe-Nanostructures-Applications-Electronics/dp/1845696891/ref=sr_1_18?ie=UTF8&qid=1289072797&sr=8-1]**

**WS: [http://www.amazon.co.uk/Hierarchical-Bipolar-Transistor-Mo delling-Hicum/dp/981427321X/ref=sr_1_18?ie=UTF8&qid=1289072797&sr=8-1]**


**WS: [http://www.amazon.co.uk/Technology-Computer-Aided-Design/dp/0863417455/ref=sr_1_18?ie=UTF8&qid=1277940142&sr=8-1]**

**WS: [http://www.amazon.co.uk/Analysis-Monolithic-Integrated-Automotive/dp/3832270876/ref=sr_1_17?ie=UTF8&qid=1277940275&sr=8-1]**
The Analysis and Design of Linear Circuits, 6th Edition
Written by Roland E. Thomas, Albert J. Rosa, Gregory J. Toussaint. Published by Wiley
The Analysis and Design of Linear Circuits, 6e gives the reader the opportunity to not only analyze, but also design and evaluate linear circuits as early as possible. The text's abundance of problems, applications, pedagogical tools, and realistic examples helps engineers develop the skills needed to solve problems, design practical alternatives, and choose the best design from several competing solutions.

Advanced Millimeter-wave Technologies: Antennas, Packaging and Circuits
Written by Duixian Liu , Ulrich Pfeiffer, Janusz Grzyb, Brian Gaucher. Published by Wiley
This book explains one of the hottest topics in wireless and electronic devices community, namely the wireless communication at mmWave frequencies, especially at the 60 GHz ISM band. It provides the reader with knowledge and techniques for mmWave antenna design, evaluation, antenna and chip packaging. WS: http://eu.wiley.com/WileyCDA/WileyTitle/productCd-047099617X.html

Modeling and Characterization of RF and Microwave Power FETs (The Cambridge RF and Microwave Engineering Series)
Written by Peter Aaen , Jaime A. Pla & John Wood, all of Freescale Semiconductor. Published by Cambridge University Press.
A book about the compact modeling of RF power FETs with descriptions of characterization and measurement techniques, analysis methods, and the simulator implementation, model verification and validation procedures that are needed to produce a transistor model that can be used with confidence by the circuit designer.

Strained-Si Heterostructure Field Effect Devices (Material Science and Engineering)
Written by C K Maiti, Published by Taylor & Francis Ltd
A combination of the materials science, manufacturing processes, and pioneering research and developments of SiGe and strained-Si have offered an unprecedented high level of performance enhancement at low manufacturing costs. Encompassing all of these areas, "Strained-Si Heterostructure Field Effect Devices" addresses the research needs associated with the front-end aspects of extending CMOS technology via strain engineering.
WS: http://www.amazon.co.uk/ref=ab_u_w_b_k?url=search-alias%3Daps&field-keywords=Strained-Si+Heterostructure+Field+Effect+Devices&Go.x=12&Go.y=8

ESD : RF Technology and Circuits
Written by Steven Howard Voldman. Published by Wiley
Electrostatic Discharge (ESD) within RF devices can result in the malfunctioning of nearby electronic equipment. This volume is designed as the third in a series of three books addressing ESD physics, devices, circuits and design. The first book to address the increasingly important area of ESD within RF devices and circuits.
WS: http://www.amazon.com/ESD+Technology-Steven-Howard-Voldman/dp/0470847557/ref=sr_1_1?ie=UTF8&qid=1161770907&sr=8-1

Thin Film Solar Cells: Fabrication, Characterization and Applications
Written by Jef Poortmans & Vladimir Arkhipov. Published by Wiley (Series in Materials for Electronic & Optoelectronic Applications)
This book aims to present for the first time an in-depth overview of this topic covering a broad range of thin-film solar cell technologies including both organic and inorganic materials, presented in a systematic fashion, by the scientific leaders in the respective domains, as well as related topics, from physical principles to design, fabrication, characterization, and applications of novel PV devices.
WS: http://www.amazon.com/Thin-Film-Solar-Cells+Characterization-As-1199914477&sr=8-4

The Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy
Written by John D. Cressler, Georgia Institute of Technology. Published by CRC PRESS
Bringing the many aspects of silicon heterostructures into one convenient resource, this handbook presents a comprehensive perspective of the field. It covers topics ranging from materials, to fabrication, to devices, to CAD, to circuits, and applications. Each chapter is written by a leading international expert, ensuring depth of coverage, up-to-date research results, and a comprehensive list of seminal references. A novel aspect of this handbook is that it contains "snap-shot" views of the industrial state-of-the-art for devices and circuits and is designed to provide the reader with a useful basis of comparison for the current status and future course of the global silicon heterostructure industry.
WS: http://www.crcpress.com

SiGe Heterojunction Bipolar Transistors
Written by P. Ashburn. Published by John Wiley & Sons Ltd.
SiGe HBTs is a hot topic within the microelectronics community because of its applications potential within integrated circuits operating at radio frequencies. Applications range from high speed optical networking to wireless communication devices. The addition of germanium to silicon technologies to form SiGe devices has created a revolution in the semiconductor industry. These transistors form the enabling devices in a wide range of products for wireless and wired communications.
WS: http://www.amazon.co.uk/exec/obidos/AEIN/0470848383/qid=1073306171sr=1-1/ref=sr_1_0?ie=UTF8&tag=6674854-20

Silicon-Germanium Heterojunction Bipolar Transistors
Written by J.D. Cressler and G. Niu. Published by Artech House, Boston, MA, USA.
This informative resource presents the first comprehensive treatment of SiGe HBTs. It offers a complete, from-the-ground-up understanding of SiGe HBT devices and technology, from a very broad perspective. The book covers motivation, history, materials, fabrication, device physics, operational principles, and circuit-level properties associated with this new cutting-edge semiconductor device technology. Including over 600 equations and more than 350 illustrations, this hands-on reference explains in clear and concise language how to design, simulate, fabricate, and measure a SiGe HBT.
WS: http://users.ece.gatech.edu/~cressler/book.html

Silicon Germanium: Technology, Modeling and Design
Written by IBM authors: Raminderpal Singh, David Harame and Modest Oprysko. Published by Wiley-IEEE Press.
"Silicon Germanium" provides detailed insight into the modelling and design automation requirements for leading-edge RF/analog and mixed-signal products. Written for RF/analogue and mixed-signal designers, CAD designers, semiconductor students, and foundry process engineers.
And finally... Goldmore releases new raindrop shaped LED toilet sensor lights

“Goldmore is excited to announce the launch of a brand new LED toilet sensor light, a rainy drop shape motion activated toilet light. Company is responding to the growing demand of the market with their invention. The official launch date of the product is 2016-10-16. Goldmore strongly believes that LED toilet sensor light will help many families to use bathroom at night without need of using disturbing flashing lights. Modern design of the product is a response to market demand and move away from the original square shape presented by their competitors. High quality materials used to manufacture the product make it stand out from current market options.”

WS: http://www.goldmore.com